UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,925	01/16/2004	Craig Hansen	43876-158	5116

7590 08/08/2008

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
MOLL, JESSE R	
ART UNIT	**PAPER NUMBER**
2181	

MAIL DATE	DELIVERY MODE
08/08/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,925	HANSEN ET AL.	
	Examiner	Art Unit	
	JESSE R. MOLL	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26 and 40-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26 and 40-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/10/07 3/24/08 6/27/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-10, 13-23 and 26 are rejected under 35 U.S.C. U.S.C. 102(b) as being anticipated by Lahti (U.S. Patent No. 4,875,161), herein referred to as Lahti'161.

Referring to claim 1, Lahti'161 discloses, as claimed, a method of processing data in a programmable processor (the system comprising scientific processor 22, see Fig. 4), the method comprising: decoding a single instruction (see Fig. 20 A, regarding decoded instruction) for selectively arranging data,

specifying a data selection operand (see Vector File address format in Fig. 13) and a first and a second register (block0 1350 and block1 1351 in Fig. 13 respectively) each having a register width, the first and second registers providing a plurality of data elements (such as words 0-63, se Fig. 13) each having an elemental width smaller than the register width, the data selection operand comprising a plurality of fields (see Col. 18, lines 30-50, regarding each field in Vector File address format) each selecting one (see Col. 18, lines 30-50, regarding an individual word is uniquely addressed) of the plurality of data elements; and for each field of the data selection operand, providing the data element (see col. 19, lines 7-63, regarding providing each word pair in each clock cycle) selected by the field to a predetermined position in a catenated result (such as Add Pipe Augend register 1318, see Fig. 13 or local store 168, see Fig. 4). Note claims 13, 14, 26, 27, and 29 recite the corresponding limitations as set forth in claim 1. As to Claims 26 and 39, Lahti'161 discloses the first register (block0 1350 in Fig. 13) providing a plurality of data elements (such as words 0, 1, 16, 17, 32, 33, 48 and 40, see Fig. 13).

As to claim 2, Lahti'161 also discloses: the method of claim 1 wherein each field of the data selection operand provides a sufficient number of bits to specify any one of the plurality of data elements (see Col. 18, lines 30-50, regarding an individual word is uniquely addressed). Note Claims 15, and 28, recite the corresponding limitations as set forth in claim 2.

As to claim 3, Lahti'161 also discloses: the method of claim 2 wherein each field of the data selection operand has a width of n bits, wherein the

plurality of data elements comprises 2^n data elements (see col. 18, lines 51-52, regarding 2^6 = 64 words are selected). Note Claims 16, and 29, recite the corresponding limitations as set forth in claim 3.

As to claim 4, Lahti'161 also discloses: the method of claim 1 wherein the data selection operand is provided by a register specified by the single instruction (the instruction for vector processing since Lahti'161's system is used for a vector processing). Note Claims 17, and 30, recite the corresponding limitations as set forth in claim 4.

As to claim 5, Lahti'161 also discloses: the method of claim 4 wherein the data selection operand (see Vector File address format in Fig. 13) has a width equal to the specified register width (the widths for word 0 and 1 in block 0, see Fig. 13 since the word width is changeable). Note Claims 18, and 31, recite the corresponding limitations as set forth in claim 5.

As to claim 6, Lahti'161 also discloses: the method of claim 1 wherein the catenated result is provided to a register (such as Add Pipe Augend register 1318, see Fig. 13 or local store 168, see Fig. 4). Note Claims 19, and 32, recite the corresponding limitations as set forth in claim 6.

As to claim 7, Lahti'161 also discloses: the method of claim 1 wherein the plurality of data elements has a combined width (the width for words 0/1 in block 0, and the width words 2/3 in block 1, see Fig. 13) equal to the width of the first register plus the width of the second register (block 0, and block 1, see Fig. 13). Note Claims 20, and 33, recite the corresponding limitations as set forth in claim 7.

As to claim 8, Lahti'161 also discloses: the method of claim 1 wherein the instruction further specifies a data element width of the plurality of data elements (such as words 0-63, see Fig. 13). Note Claims 21, and 34, recite the corresponding limitations as set forth in claim 8.

As to claim 9, Lahti'161 also discloses: the method of claim 1 wherein each data element has a width of 8 bits (note each word can be 8 bits in length). Note Claims 22, and 35, recite the corresponding limitations as set forth in claim 9.

As to claim 10, Lahti'161 also discloses: the method of claim 1 wherein the catenated result has a width of 128 bits (note each word can be 8 bits in length, therefore, the catenated result has a width of 8x16=128 bits when all the first pass in each block is transferred to the catenated result, see col. 19, lines 7-63, regarding providing each word pair in each clock cycle). Note Claims 23, and 36, recite the corresponding limitations as set forth in claim 10.

3. Claims 1, 11, 12, 14, 24 and 25 are rejected under 35 U.S.C. U.S.C. 102(e) as being anticipated by Lee (U.S. Patent No. 6,381,690).

Referring to claim 1 and 14, Lee discloses, as claimed, a method of processing data in a programmable processor the method comprising: decoding a single instruction (performed in figure 1) for selectively arranging data,

specifying a data selection operand (Order word 26; see figure 1) and a first and a second register (Items 1-2 and Items 3-4; see figure 1) each having a register width (inherently, registers have a width), the first and second registers providing a plurality of data elements (Items 1-4) each having an elemental width smaller than the register width (inherently, parts are smaller than the whole), the data selection operand comprising a plurality of fields (see figure 1 regarding the 4 sections of Order Word) each selecting one (using multiplexers 41-44; see figure 2) of the plurality of data elements; and for each field of the data selection operand (O1-O4; see figure 2), providing the data element selected by the field to a predetermined position in a catenated result (O1 selects T1, O2 selects T2,, etc…; see figure 2)

Referring to claims 11 and 24, Lee also discloses that for each field of the data selection operand, a relative location of the field within the data selection operand corresponds to a relative location of the predetermined position within the catenated result (O1 selects T1, O2 selects T2,, etc…; see figure 2).

4. Claims 40-47,49-50, 54-61 and 63-64 are rejected under 35 U.S.C. U.S.C. 102(b) as being anticipated by Cray (U.S. Patent No. 4,128,880).

Regarding claim 40, Cray discloses a method of processing data in a programmable processor, the method comprising: decoding a single instruction (Vector merge operation; see col. 6, lines 42-55) specifying a plurality of registers (Vj and Vk; see col. 6, lines 46-49) storing a plurality of 8-bit data elements (Segments of each 64-bit register part; see col. 3, lines 59-61; *Note that the term*

data element is extremely broad and a section of each register is an element.), an index register storing an index vector comprising a plurality of equal-sized (1-bit) selectors stored in partitioned fields of the index register(VM Register; see col. 6, lines 32-41) and a destination register (Vi; see col. 6, lines 49-52); and for each selector in the index vector, providing a data element selected by the selector (either from Vj or Vk; see col. 6, lines 49-51) to a predetermined position (the same position the section is stored in the source register) in the destination register.

Regarding claim 41, Cray also discloses the plurality of registers comprises two registers (Vj and Vk; additionally, any plurality of registers will inherently comprise two registers since it is a plurality).

Regarding claim 42, Cray also discloses the plurality of registers comprise two 64-bit registers storing a combined total of sixteen 8-bit data elements (see col. 3, lines 56-61; *Note that since there are more than 128 bits contained within these registers, the registers include two 64-bit registers which can be sectioned into sixteen 8-bit registers. The notation used to describe the partitioning is irrelevant, since the physical structure of these registers is merely a plurality of stored 0s and 1s.*).

Regarding claim 43, Cray also discloses the number of selectors stored in the index register is equal to the number of predetermined positions in the destination register (64; see col. 3, line 59; col. 6, line 32).

Regarding claim 44, Cray also discloses the index register is a 64-bit register (see col. 6, line 32).

Regarding claim 45, Cray also discloses the index vector comprises n (64) equal sized (1-bit) selectors (see col. 6, line 32) and the destination register comprises n (64) equal-sized (64-bit) predetermined positions (see col. 3, lines 59).

Regarding claim 46, Cray also discloses the selector stored in a lowest order set of bits of the index register provides a data element to a lowest order set of bits of the destination register, the selector in a second lowest order set of bits of the index register provide a data element to a second lowest order set of bits of the destination register and the selector stored in a highest order set of bits of the index register provides a data element to a highest order set of bits of the destination register (see col. 6, lines 51-55; " If bit n of the vector mask is one, the first of the nth ordered operands is transmitted; if bit n of the mask is 0, the second of the nth ordered operands (the nth Vk element) is selected and transmitted to the nth element of the Vi register").

Regarding claim 47, Cray also discloses the destination register is a 128-bit register.

Regarding claim 49, Cray also discloses the index register stores sixteen 4-b selectors (see col. 6, line 32; *Note that each group of 4 selector bits is a selector because it selects 4 pieces of data*).

Regarding claim 50, Cray discloses a method of processing data in a programmable processor, the method comprising: decoding a single instruction (Vector merge operation; see col. 6, lines 42-55) specifying a plurality of registers (Vj and Vk; see col. 6, lines 46-49) storing a plurality of 8-bit data elements (Segments of each 64-bit register part; see col. 3, lines 59-61; *Note that the term data element is extremely broad and a section of each register is an element.),* an index register storing an index vector comprising a plurality of equal-sized (1-bit) selectors stored in partitioned fields of the index register(VM Register; see col. 6, lines 32-41) and a destination register (Vi; see col. 6, lines 49-52); and for each selector in the index vector, providing a data element selected by the selector (either from Vj or Vk; see col. 6, lines 49-51) to a predetermined posisiton (the same position the section is stored in the source register) in the destination register.

Claims 54-61 and 63-64 recite equivalent limitations as claims 40-47 and 49-50 and are rejected under the same grounds.

\

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Matsuura (US Patent No. 4,725,973) herein referred to as Matsuura.

Referring to claims 12 and 25, Lee does not expressly disclose decoding a second single instruction specifying a third and a fourth register each containing a plurality of floating-point operands; multiplying the' plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality or of products; and providing the plurality of products to partitioned fields of a result register as a catenated result.

Matsuura teaches decoding a second single instruction (Vector Multiply) specifying a third (VR 1) and a fourth register (VR 1); multiplying the' plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality or of products; and providing the plurality of

products to partitioned fields of a result register (VR 3) as a catenated result (See col. 2, lines 5-20).

At the time of the invention, it would have been obvious for one of ordinary skill in the art to have modified the invention of Lee by using a Vector multiply instruction, as taught by Matsuura, resulting in predictable results for the purpose of increasing flexibility and performance of SIMD processing.

6. Claims 40, 48, 50-53, 54, 62 and 64-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blelloch (Vector Models for Data-Parallel Computing) in view of In re Rose, 105 USPQ 237 (CCPA 1955).

Regarding claims 40 and 54 Blelloch discloses a method of processing data in a programmable processor, the method comprising: decoding a single instruction (Permute instruction, see page 62) specifying a plurality of registers (First half of data vector and Second half of data vector; see page 62) storing a plurality of elements (Segments of Data vector storing A0-A7*),* an index register storing an index vector (Index Vector; see [age 62) comprising a plurality of selectors stored in partitioned fields of the index register (each selector in the index vector) and a destination register (C; see page 62); and for each selector in the index vector, providing a data element selected by the selector (see page 62, section 4.1.3 regarding rearranging elements) to a predetermined position (one of the 8 positions) in the destination register.

Regarding claims 50-53 and 64-67 Blelloch discloses A method of processing data in a programmable processor, the method comprising: decoding a single instruction (Permute instruction, see page 62) specifying a first register (First half of data vector) storing a first plurality of data elements (A0-A3), a second register (Second half of data vector; see page 62) storing a second plurality data elements (A4-A7), an index register storing an index vector (Index Vector; see page 62) comprising a plurality of selectors stored in partitioned fields (each selector in the index vector) of the index register and a destination register (C); for each selector in the index vector, providing a data element from one of the first or second plurality of data elements (see page 62, section 4.1.3 regarding rearranging elements) selected by the selector to a predetermined position in the destination register (one of the 8 positions), wherein the predetermined positions are contiguous blocks of bits that take up an entire width of the destination register (see both figures on page 62)

Blelloch does not expressly disclose the data elements and the predetermined positions are 8-bit (Claims 50 and 64), the selectors are equal-sized (Claims 50 and 64) 4-bit elements (Claims 48, 53, 62 and 67), the first and second registers are 64-bit registers (Claims 51 and 65), the index register is 64-bit (Claims 51 and 65) and the destination register is 128-bit (Claims 52 and 66).

In re Rose has shown that changes in size, such as change in the size of the data, is not generally given patentable weight or would have been obvious improvements. Hence, it would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the invention of Blelloch, by making the predetermined positions 8-bit, the selectors equal-sized 4-bit elements, the first and second registers 64-bit registers, the index register 64-bit and the destination register 128-bit, as in re rose has shown to be obvious.

MPEP 2141 reads, in part, as follows:

> The Supreme Court in KSR reaffirmed the familiar framework for determining obviousness as set forth in Graham v. John Deere Co. (383 U.S. 1, 148 USPQ 459 (1966)), but stated that the Federal Circuit had erred by applying the teaching- suggestion-motivation (TSM) test in an overly rigid and formalistic way. KSR, 550 U.S. at, 82 USPQ2d at 1391. Specifically, the Supreme Court stated that the Federal Circuit had erred in four ways: (1) "by holding that courts and patent examiners should look only to the problem the patentee was trying to solve" (Id. at__ 82 USPQ2d at 1397); (2) by assuming "that a person of ordinary skill attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem" (Id.); (3) by concluding "that a patent claim cannot be proved obvious merely by showing that the combination of elements was obvious to try'" (Id.); and (4) by overemphasizing "the risk of courts and patent examiners falling prey to hindsight bias" and as a result applying "[r]igid preventative rules that deny factflnders recourse to common sense" (Id.).
>
> In KSR, the Supreme Court particularly emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," Id, at__82 USPQ2d at 1395, and discussed circumstances in which a patent might be determined to be obvious. Importantly, the Supreme Court reaffirmed principles based on its precedent that "the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. "Id, at__82 USPQ2d at 1395.

The Supreme Court further stated that:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his ordinary skill. Id. at__82 USPQ2d at 1396. When considering obviousness of a combination of known elements, the operative question is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." Id. at__82 USPQ2d at 1396.

All the elements necessary to produce applicants' invention were known in the art. How one combined such elements to produce applicants' invention was also known in the art. Evidence of this is that applicants' disclosure lacks any detailed description of unique technology necessary to implement applicants' invention. One of ordinary skill would have readily recognized that the results of the combination were predictable. Absent some secondary considerations, not in evidence at this time, applicants invention is obvious over the combination of prior art presented.

Claims 64-67 recite equivalent limitations as 50-53 and are rejected under the same grounds.

Response to Arguments

7. Applicant's arguments with respect to the rejection under 35 USC 101 have been fully considered and are persuasive. The rejection of the claims under 35 USC 101 has been withdrawn.

8. Applicant's arguments, filed 25 January 2007, with respect to the rejection under 35 USC 101 have been fully considered and are persuasive. The rejection of these claims has been withdrawn.

9. Applicant's arguments filed 25 January 2007, with respect to the rejection under 35 USC 102 have been fully considered but they are not persuasive.

Applicant states:

> Lahti fails to disclose such a data selection operand. Instead, Lahti discloses a conventional memory address format comprising a plurality of fields that must be read together to select one word of data.

Examiner disagrees. Clearly, any address is a data selection operand, since an address is merely a number selecting a location in memory.

Regarding the arguments directed to the limitation "each selecting one of the plurality of data elements," Examiner disagrees. Nowhere in the prior Office Action is it stated that individual fields used individually to select a word from Lahti's memory space. In fact, each field together MUST be used (as admitted

by applicant) to "provid[e] the data element selected by the field". The claim does not require that each field be able to select an element by itself, but merely requires the that each field select an element. Since each element is used to select a piece of data, the system of Lahti falls under the claim language.

Regarding claim 2, Examiner disagrees. Again, the claim does not require that each field have enough bits to independently select any element, and therefore since each field can select any element when combined with the other fields, it falls under the claim limitations of claim 2.

Regarding claim 3, Examiner disagrees. The term field is a very broad term and any arrangement of bits is a field. Therefore, if the address is considered to be segmented (the bits need not be physically separated) into 6 bit segments, each segment is considered to be a field. These segments are each used together to select data elements.

Regarding claim 5, Examiner disagrees. Like above, word is an extremely broad term. A word is merely a group of bits in a computer. A register is merely a set of 12-bit words.

Regarding claim 8, Examiner disagrees. Inherently, an instruction must specify a width. An operation cannot occur on an undetermined amount of data.

Any instruction clearly points out what computations must be done, and on which data. The amount of data to be computed is a width.

Regarding claim 9, see above regarding claims 3 and 5.

Conclusion

10. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 24 March 2008 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSE R. MOLL whose telephone number is

(571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

/J. R. M./
Examiner, Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181